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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,027	09/22/2003	Takahiko Hara	81790.0299	1423
26021	7590	03/03/2005	EXAMINER	
HOGAN & HARTSON L.L.P. 500 S. GRAND AVENUE SUITE 1900 LOS ANGELES, CA 90071-2611			LE, VU ANH	
			ART UNIT	PAPER NUMBER
			2824	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

**Office Action Summary**

Application No.

10/668,027

Applicant(s)

HARA ET AL.

Examiner

Vu A. Le

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,4,5,8,10,13 and 18 is/are rejected.
- 7) ☒ Claim(s) 2,3,6,7,9,11,12 and 14-17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>09/22/03</u> . | 6) <input type="checkbox"/> Other: ____.  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4-5, 8, 10 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Sekiguchi et al (6,477,100).

Sekiguchi et al (Fig.3) disclose a semiconductor integrated circuit comprising: a memory cell array (Array) having memory cells arranged in matrix form; sense amplifiers (SA) which amplify a signal read out from the memory cells and which include N channel sense amplifiers (Q5 and Q6) each comprising an N channel MOS transistor and P channel sense amplifiers (Q7 and Q8) each comprising a P channel MOS transistor; a first and second drive circuits (Q3 and Q4) each including an N channel MOS transistor which drives the N channel sense amplifiers or P channel amplifier respectively, included in the sense amplifiers, the first and second drive circuits being arranged adjacent to the sense amplifiers; and a sense amplifier control circuit (inherent) which supplies a

common control signal to both gate electrodes of the N channel MOS transistors included in the first and second drive circuits.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sekiguchi et al in view of Ooishi.

5. Claim 18 recites a feature of an equalize circuit for equalizing a source potential at the N channel MOS transistor constituting the N channel sense amplifier with a source potential at the P channel MOS transistor constituting the P channel sense amplifier. Sekiguchi et al fails to disclose this feature. However, Ooishi discloses an equalize circuit for a sense amplifier as recited in claim 18. Therefore, it would have been obvious to one of ordinary skill in the art at the time this invention was made to modify Sekiguchi et al by adding an equalize circuit for a sense amplifier as disclosed by Ooishi to increase the sensing speed.

***Allowable Subject Matter***

6. Claims 2-3, 6-7, 9, 11-12, and 14-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-3, 6-7, 9, 11-12, and 14-17 disclose allowable features such as P channel sense amplifier being formed on an N type well area, N channel sense amplifier being formed on an P type well area, a transistor size ratio of an N channel MOS transistor possessed by the first driving circuit and N channel MOS transistor possessed by the second driving circuit being set by changing the numbers of the first and second circuit groups arranged to change the numbers of first and second driving circuits, gate length of the N channel MOS transistor included in the first drive circuit is equal to a gate length of the N channel MOS transistor included in the second drive circuit.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Matsumoto (6,466,502) discloses a semiconductor memory device having switching and memory cell transistors with the memory cell having the lower threshold voltage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Vu A. Le  
Primary Examiner  
Art Unit 2824

03/01/05